We claim:

1. A circuit configuration in switched op-amp technology, comprising:

at least one switchable operational amplifier having an input and an output;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a clock generator producing at least two non-overlapping switching-clock signals each having switching-clock phases including an on-phase and an off-phase;

said at least two non-overlapping switching-clock signals including a first switching-clock signal and a second switching-clock signal;

said clock generator controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

a phase-variance device varying said switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance device connected to said clock generator.

2. The circuit configuration according to claim 1, wherein said phase-variance device is configured to vary each of said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

3. The circuit configuration according to claim 1, wherein said phase-variance device is configured to vary each second one of said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

4. The circuit configuration according to claim 1, wherein:

said operational amplifier has a transient response; and

said phase-variance device is configured to vary a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said transient response of said operational amplifier.

5. The circuit configuration according to claim 1, wherein:

said operational amplifier has transistors having a switching speed; and

said phase-variance device is configured to vary a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon said switching speed of said transistors.

6. The circuit configuration according to claim 5, including a detector for detecting said switching speed of said transistors, said detector connected to said operational amplifier.

7. The circuit configuration according to claim 6, wherein:

said transistors include at least one of:

n-channel FETs; and

p-channel FETs;

said transistors each have a respective switching speed; and

said detector separately detects said switching speed of said n-channel FETs and said p-channel FETs.

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8. The circuit configuration according to claim 6, including an inverter chain, said detector having one of:

an XOR gate with XOR inputs, one of said XOR inputs receiving an undelayed edge signal, and another of said XOR inputs receiving an edge signal delayed through said inverter chain; and

an XNOR gate with XNOR inputs, one of said XNOR inputs receiving an undelayed edge signal and another of said XNOR inputs receiving an edge signal delayed through said inverter chain.

9. The circuit configuration according to claim 6, wherein said detector generates detector pulses having a duration characterizing said switching speed of said transistors.

10. The circuit configuration according to claim 9, wherein said phase-variance device is configured to adjust a duration of said switching-clock phases in which said first and second switching-clock signals are in said off-phase dependent upon a duration of said detector pulses.

11. The circuit configuration according to claim 1, wherein said phase-variance device is configured to adjust a duration of said switching-clock phases in which said first and second

switching-clock signals are in said off-phase in a given number of predetermined steps.

12. The circuit configuration according to claim 1, wherein said clock generator and said phase-variance device are embodied as a programmable clock generator.

13. The circuit configuration according to claim 1, wherein said clock generator and said phase-variance device are embodied as:

an external squarewave generator producing a squarewave signal; and

a divider circuit connected to said squarewave generator, said divider circuit generating said at least two switching-clock signals from said squarewave signal.

14. The circuit configuration according to claim 13, wherein:

said squarewave signal has a duty ratio; and

adjustment of said duty ratio varies said switching-clock phases in which said first and second switching-clock signals are in said off-phase.

15. A circuit configuration in fully differential circuit technology, comprising:

at least one switchable operational amplifier having an input and an output;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a clock generator producing at least two non-overlapping switching-clock signals each having switching-clock phases including an on-phase and an off-phase;

said at least two non-overlapping switching-clock signals including a first switching-clock signal and a second switching-clock signal;

said clock generator controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

a phase-variance device varying said switching-clock phases in which said first and second switching-clock signals are in

said off-phase, said phase-variance device connected to said clock generator.

16. A circuit configuration in switched op-amp technology, comprising:

at least one switchable operational amplifier having an input and an output;

at least one sampling capacitor connected to said input;

at least one integrating capacitor connected to said input and to said output;

a means for generating at least two non-overlapping switching-clock signals each having and on-phase and an off-phase;

said at least two non-overlapping switching-clock signals including a first switching-clock signal and a second switching-clock signal;

said clock generator means controlling charging of said sampling capacitor with said first switching-clock signal and switching said operational amplifier on and off with said second switching-clock signal; and

a means for varying switching-clock phases in which said first and second switching-clock signals are in said off-phase, said phase-variance means connected to said clock generator means.

17. A method for clocking successive operational amplifier stages constructed in switched op-amp technology, which comprises:

generating at least two non-overlapping switching-clock signals;

switching a first operational amplifier on and off with a first signal of the two switching-clock signals;

switching a second operational amplifier on and off with a second signal of the switching-clock signals; and

varying switching-clock phases in which the operational amplifiers are switched off.

18. The method according to claim 17, which further comprises varying each of the switching-clock phases in which the operational amplifiers are switched off.

19. The method according to claim 17, which further comprises varying each second one of the switching-clock phases in which the operational amplifiers are switched off.

20. The method according to claim 17, which further comprises varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a transient response of the operational amplifiers.

21. The method according to claim 17, which further comprises varying a duration of the switching-clock phases in which the operational amplifiers are switched off dependent on a switching speed of transistors of the operational amplifiers.

22. The method according to claim 17, which further comprises separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs.

23. The method according to claim 21, which further comprises separately detecting at least one of a switching speed of n-channel FETs and a switching speed of p-channel FETs.

24. The method according to claim 17, which further comprises adjusting a duration of the switching-clock phases in which the operational amplifiers are switched off in a number of predetermined steps.

25. The method according to claim 17, which further comprises generating the at least two non-overlapping switching-clock signals with a programmable clock generator.

26. The method according to claim 17, which further comprises generating the at least two non-overlapping switching-clock signals with an external squarewave generator and a divider circuit.

27. The method according to claim 26, which further comprises varying the switching-clock phases in which the operational amplifiers are switched off by adjusting a duty ratio of a squarewave signal from the squarewave generator.